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THE DC-FAULT BLOCKING CAPABILITY BY A NEW HYBRID MULTILEVEL CONVERTER IN HVDC TRANSMISSION

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ABSTRACT: This paper investigates the performance of new multilevel converter topology intended for HVDC applications, called the cascaded H-bridge and arm converter. It is a hybrid between the modular multilevel converter and the two level converters. The proposed converter offers current limiting capability during dc-side fault. This feature eliminates the need of dc-side circuit breakers in dc power transmission system and filter design by generating higher pulse level. A simplified proposed converter steady state model is first developed that can be used for power flow analysis. The transient performance is analyzed by examining the proposed system responses to external AC-side and DC-side faults. Furthermore, the proposed converter can keep control of the current in the phase reactor even in case of a dc-side fault and support the ac grid. Simulation results and loss calculations are presented in this paper in order to support the claimed features of the proposed converter.

KEYWORDS: Multilevel converter, power system faults, fault tolerance, cascaded H-bridge arm converter.

1. INTRODUCTION

The introduction of voltage source converter technology into high-voltage DC (HVDC) transmission systems has increased their growth and development in many applications[1]. The main benefits of voltage-source-converter high voltage dc (VSC-HVDC) over the classic line commutated converter based HVDC (LCCHVDC) are [2]-[3]:

- Converter inherent reactive power capability.
- Independent control of active and reactive Power.
- Black start capability of HVDC system.
- Without need to reverse the DC link voltage polarity, power reversal is achieved instantaneously.
- Improved ac fault ride-through capability and the unique feature of current-limiting during dc side faults (pole to pole fault).
- In the last decade, VSC-HVDC transmission systems have evolved from simple two-level converters to the multilevel converters such as modular converters [4].

This paper presents the analysis of a new converter topology, which is part of a new generation of VSCs [4], [5], based on the multilevel approach but also takes some characteristics from the two-level VSC. As explained through this paper, one of the features of this topology lies in its ability to retain control of the phase current during the loss of the dc-bus voltage, thanks to the presence of cascaded H-bridge cells in the ac side. The key advantage of this new topology lies in its reduced number of cells; thus, it does not compromise the efficiency of the converter, nor on the number of devices and even saves volume because of the reduced number of cells per arm. A component level simulation of a converter is used to confirm the claimed characteristics of this new topology. Notwithstanding the advantages brought by this new generation of converters, there are some aspects that can still be improved. The avoidance of the ac filter means that the cells are now one of the bulkiest components of the converter station and cell format requires a physically large capacitor in addition to the set of IGBTs. Half-bridge cells are normally used in preference to H-bridge cells (both illustrated in Fig. 1 in order to reduce the number of devices in conduction at any time and, therefore, reduce the conduction power loss. Even if this choice is justified by the large cost associated with the power losses, it also means that the converter is vulnerable to a dc-side fault in a similar way to a two-level converter whereas an H-bridge version would not be. With coordination between the two level converter and cascaded H-Bridge cells in the ac -side, the dc fault

reverse-blocking capability of the hybrid converter is exploited to achieve the following:
i. during dc fault period eliminate the ac grid contribution with dc system, hence minimizing the risk of converter failure due to uncontrolled over current.
ii. Facilitate controlled recovery without interruption of the VSC-HVDC system from dc-side faults without the need for opening ac-side circuit breakers.
iii. During dc-side faults, improve voltage stability of the ac networks by converter reactive power consumption is reduced.
iv. Simplify dc circuit breaker design due to a reduction in the magnitude and duration of the dc fault current.

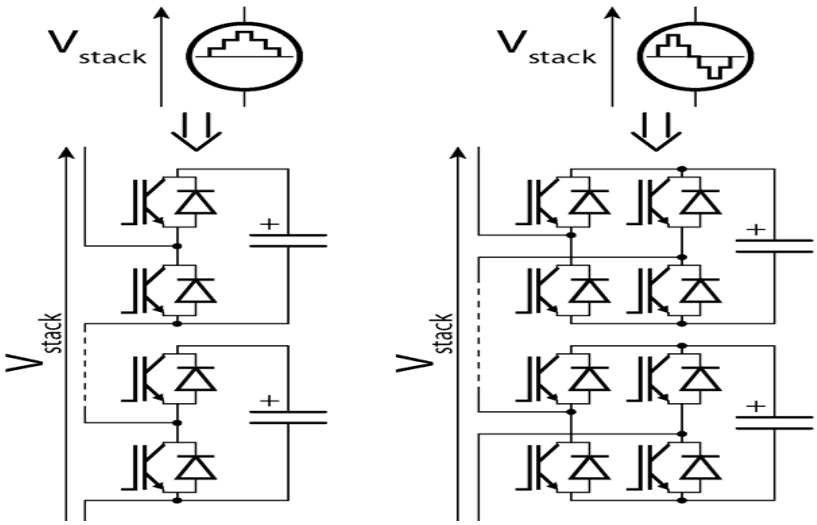


Figure 1: Schematic of half-bridge cells (left) and H- Bridge cells (right)

2. PROPOSED CONVERTER TOPOLOGY

2.1 Operation

Briefly presented in [6], proposed converter is a hybrid topology which combines features of the multilevel and two level converter topologies. As illustrated in Fig. 3, each phase of the converter consists of two arms, each with a director switch, a small arm inductor and H-bridges are cascaded in ac-side. The stack of H-bridge cells is responsible for the multistep voltage generation, as in a modular multilevel converter. Since H-bridge cells are used, the voltage produced by the stack can be either positive or negative. The proposed converter is able to produce its ac voltage higher than the dc terminal voltage if required. The director switch is composed of IGBTs connected in series in order to withstand the maximum voltage which could be applied across the director switch when it is in the open state. The main role of this director switch is to determine which arm is used to conduct the ac current. The main feature of this topology is to use essentially one arm per half cycle to produce the ac voltage. By using the upper arm to construct the positive half-cycle of the ac sine wave and the lower arm for the negative part, the maximum voltage that each stack of cells has to produce is equal to half of the dc bus voltage, which is approximately half the rating of the arm of the MMC. The resulting voltage and current waveforms of the cells and reactor switches are illustrated in Fig. 2.
The aim of the proposed converter is to reduce the number of cells, hence the volume and losses of the converter station. The short period of time when one arm finishes its working period and hands over conduction of the phase current to the opposite arm is called the overlap period. Since each arm has an active stack of cells, it can fully control the arm current to zero before opening the director switch, hence achieving soft-switching of the director switch, further lowering the power losses.

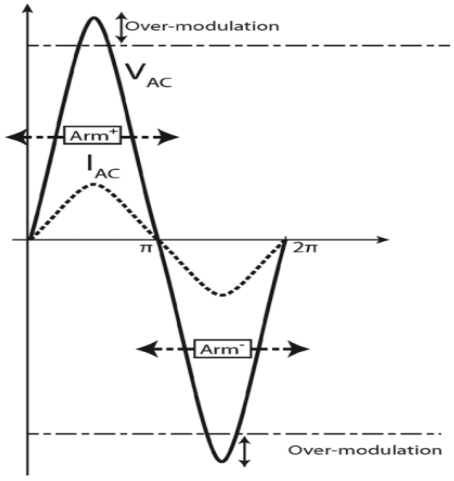


Figure 2: Idealized voltage and current wave
Waveforms over one cycle in a phase

Although normally short, the overlap period can provide additional control features, such as controlling the amount of energy stored in the stacks H-bridge cells, as explained in Section II-B.

2.2 Energy Balance

The ability of the proposed converter to generate fine voltage steps comes from its H- bridge cells, specifically, from the charged capacitors inside the H-bridges. Since the resulting ac current from system is flowing through them, the charge on the H-bridge cell capacitors will fluctuate over finite time. These fluctuations are depending on the switching states of the cell and the direction of the current. Because of large number of cells is used, amount of energy which is stored by the cells as a whole. Assuming that this charge in the H-bridge cells is evenly distributed among the various H- bridge cells, thanks to some rotation mechanisms by controlling switches, the only requirement left to ensure satisfactory operation of the proposed converter is to keep the energy of the stacks close to their nominal value. To achieve this, the converter has to be operated in such way that the net energy exchange for the stacks over each half cycle is strictly zero. Based on the below functions (1) of $V_{AC}(t)$ and $I_{AC}(t)$

$$V_{\mathrm{AC}}(t) = \hat{V}_{\mathrm{AC}} \sin(\omega t)$$
$$I_{\mathrm{AC}}(t) = \hat{I}_{\mathrm{AC}} \sin(\omega t + \phi_{\mathrm{AC}}). \qquad (1)$$

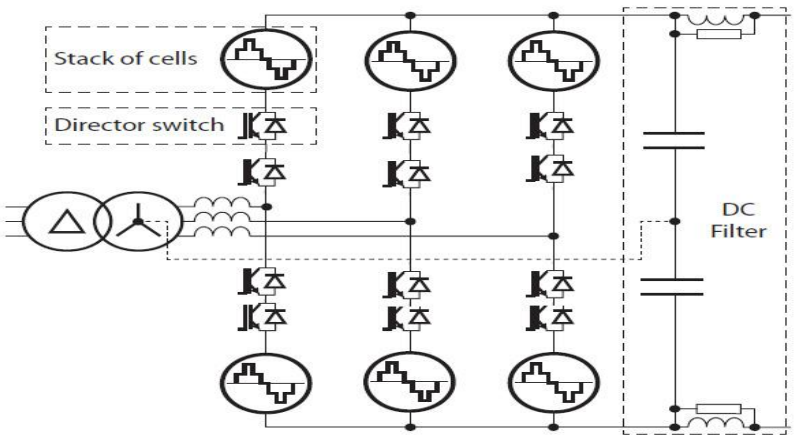


Figure: 3 Schematic of the cascaded H-bridge and arm converter, with the optional middle-point connection shown in a dashed line.

The energy exchange corresponds to the difference between the amount of energy coming from the ac side (2) and going to the dc side (3)

$$E_{\mathrm{AC}} = \int_0^{\frac{T}{2}} V_{\mathrm{AC}}(t) I_{\mathrm{AC}}(t) dt$$
$$= \frac{\hat{V}_{\mathrm{AC}} \hat{I}_{\mathrm{AC}} cos(\phi_{\mathrm{AC}}) T}{4} \quad (2)$$

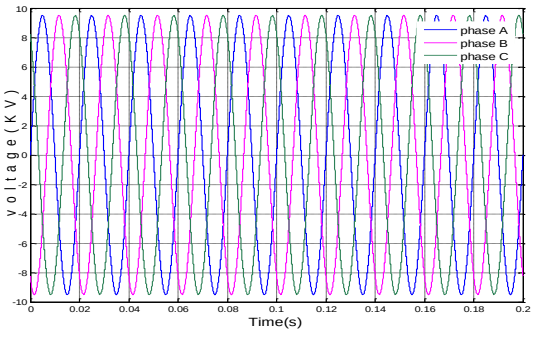
$$E_{\mathrm{DC}} = \int_0^{\frac{T}{2}} \frac{V_{\mathrm{DC}}}{2} I_{\mathrm{AC}}(t) dt$$
$$= \frac{V_{\mathrm{DC}} \hat{I}_{\mathrm{AC}} cos(\phi_{\mathrm{AC}}) T}{2\pi}. \quad (3)$$

The converter is thus required to generate its ac voltage in over modulation mode, at a level of approximately 27% higher than the dc terminal voltage. The presence cells in the proposed converter are thus fully justified since these cells are generating a negative voltage, thus pushing the voltage higher than the dc terminal voltage by 27%. By choosing the turns ratio of the power transformer between the ac grid and the converter in order to obtain the ac voltage at required level, the converted energy will flow through the converter without a deficit or surplus being exchanged with the stacks. In practice, discrepancies between the converter and its theoretical model will lead to a small fraction of the converted energy being exchanged with the stack. To remedy this, the overlap period (i.e., the small period of time when one arm hands over conduction of the phase current to the other arm) can be used to run a small dc current through both arms to the dc side. This will result in an exchange of energy between the H- bridge cell stacks and the dc capacitor, which can be used to balance the energy in the H-bridge cell stacks.

3. PERFORMANCE EVALUATION

3.1 Performance under normal conditions

The behavior of the proposed converter was simulated under normal operating conditions in order to test its performance. In this section, the converter is running in rectifier operation mode(AC to DC), converting 20MW and providing 5-MVAr capacitive reactive power. Fig. 4 shows the waveforms generated by the proposed converter in this simulation. The waveform of the phase current in the ac grid connection is high quality with only very low amplitude harmonics. Third, the dc current exhibits the characteristic six-pulse ripple inherent in the rectification method of this converter, but attenuated by an inductor placed between the converter and the dc grid. Fourth, this rectification action of the current is particularly observable in the fourth graph which shows the arm currents in phase A, indicating when an arm is conducting. Finally, the fifth graph presents the average voltage of the cells in both stacks of phase A, with their off state voltage being controlled to stay at the reference value of 1.5 kV. The voltage and current waveforms have been post processed together with the switching commands sent to the converter from the controller, in order to determine the generated power losses.



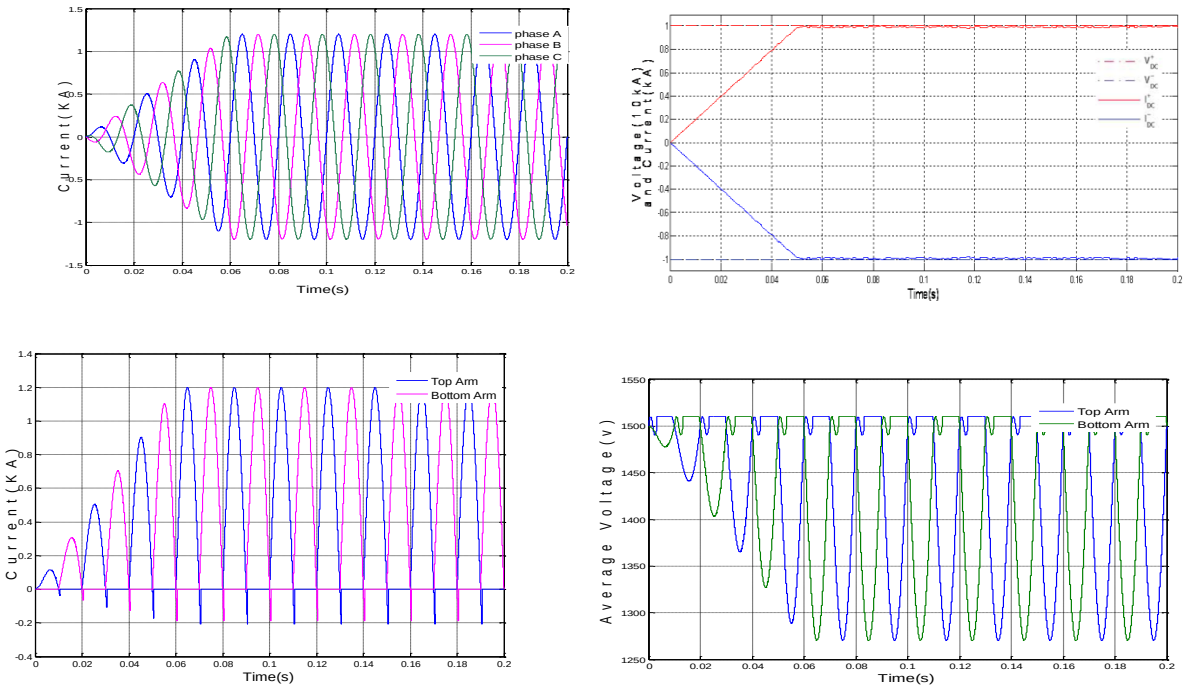


Figure: 4 Simulation results of a proposed model running in rectifier mode under normal conditions.

3.2 Robustness against AC Faults

Since the AAC is a type of VSC, it does not rely on a strong ac voltage to operate. As a consequence, the AAC is able to cope with ac-side faults. Fig. 5 shows the results of the simulation where the ac voltage drops to 0.3-p.u. retained voltage between 0.20 and 0.35 s, similar to a major fault on the ac grid. The converter switches into voltage-control mode and supplies 1.0-p.u.

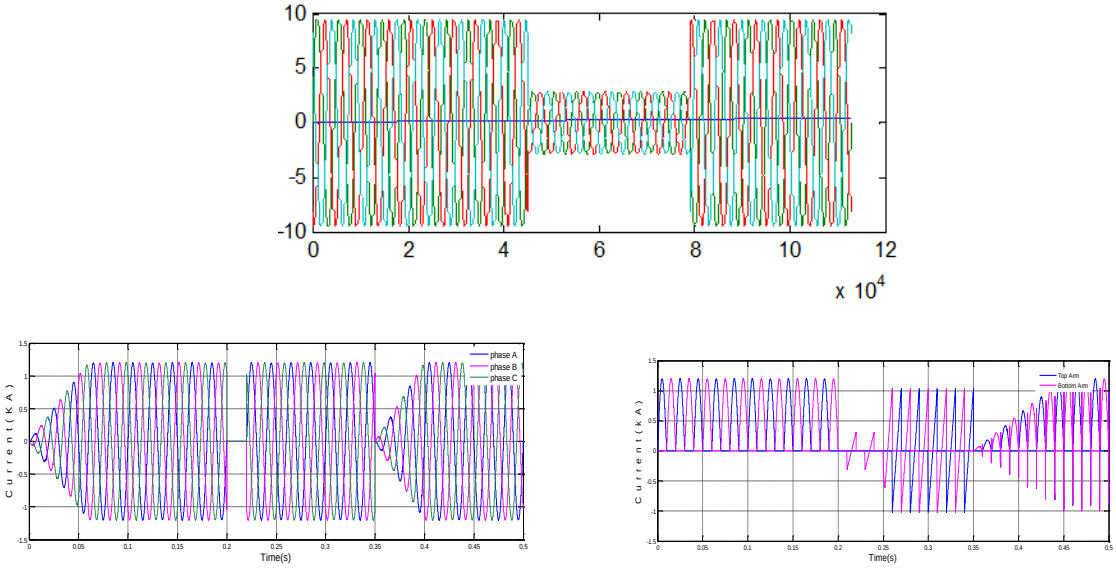


Figure: 5 Simulation results of a 20-MW AAC model running in rectifier mode when an ac-side fault occurs between 0.20 and 0.35 s.

3.3 DC Fault Blocking Capability

The intended ability to block current during dc faults was tested by simulating the temporary reduction of the dc bus voltage to zero, equivalent to a dc-side fault. The graph in Fig. 6 shows the waveforms generated during this simulation, where the dc bus voltage is lost between 0.20 and 0.35 s followed by a ramp up back to normal operations.

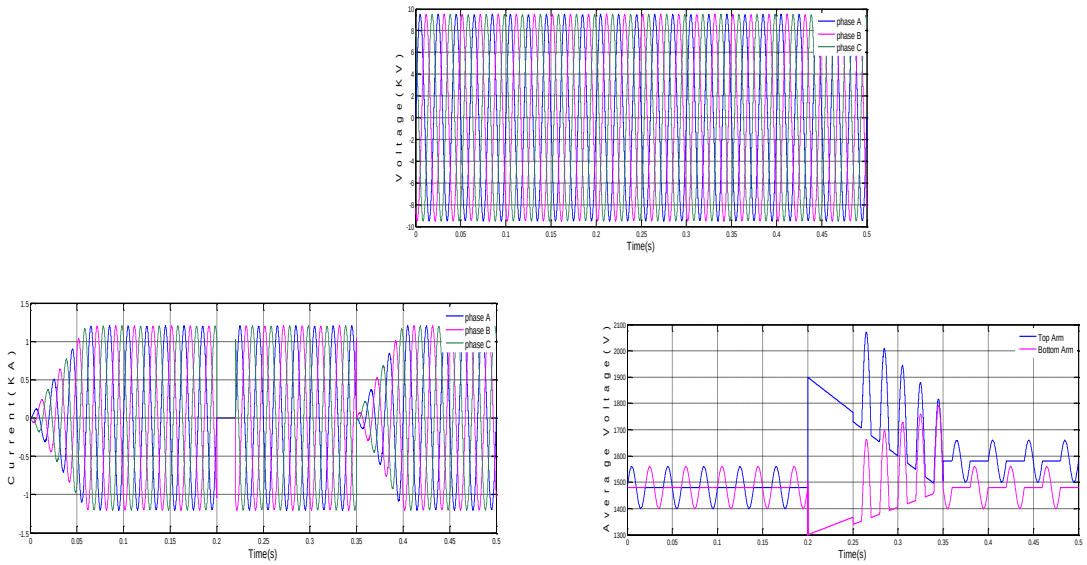


Figure: 6 Simulation results of a proposed model running in rectifier mode when a dc-side fault occurs between 0.20 and 0.35 s.

4. CONCLUSION

The proposed converter is a hybrid topology between the two-level converter and the modular multilevel converter. By combining stacks of H-bridge cells with director switches, it is able to generate almost harmonic-free ac current, as does the modular multilevel approach. And by activating only one arm per half cycle, like the two-level converter, it can be built with fewer cells than the MMC. Since this topology includes cells with capacitors which are switched into the current path, special attention needs to be paid to keeping their stored energy (equivalently, the cell capacitor voltage) from drifting away from their nominal value. A discussion of the total number of devices required by this topology has also been presented. Providing dc fault blocking and overlap both require more than the bare minimum number of cells and adding cells does lead to increased conduction power loss which gives rise to a design tradeoff.

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